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**HIGH RESOLUTION PWM GENERATOR OR DIGITALLY
CONTROLLED OSCILLATOR**

This invention relates to oscillators, and in the preferred embodiment, an
5 improved method and apparatus for use in Pulse Width Modulation (PWM) and
Digitally Controlled Oscillator (DCO) circuits. The invention has particular
applicability in areas where it is desired to increase the resolution of a PWM or DCO
without increasing the clock speed.

PWM and DCO circuits are used in a variety of applications, including, for example
10 lamp drivers. Such circuits usually utilize a counter having a clock input to generate on and
off time periods in an output signal. Typically, the contents of the register are compared
with a counter, and the counter is reset each time it reaches the value stored in the register.

The time resolution of the PWM circuit depends upon the clock frequency. A very
high clock frequency results in an improved time resolution. However, increased
15 frequencies of the clock lead to higher power consumption and electromagnetic interference
(EMI). Additionally, the integrated circuit (IC) fabrication processes to produce ICs that
can operate as such high frequencies are significantly more expensive than their lower
frequency counterparts.

Accordingly, there is a need in the art for an improved technique for achieving
20 relatively high time resolution with a relatively low clock signal for use in PWM and DCO
circuits.

Figure 1 depicts a conventional prior art implementation of a PWM or DCO
generator;

Figure 2 shows a schematic of a DCO generator using a relatively low clock rate
25 and relatively high time resolution in accordance with the invention;

Figure 3 depicts plural waveforms showing the time resolution resulting from the
arrangement of Figure 2;

Figure 4 depicts an exemplary embodiment of the invention for generating a
PWM signal with relatively high time resolution; and

30 Figure 5 depicts several graphs showing the relatively high time resolution of the
arrangement of Figure 4.

Figure 2 shows a DCO generator with improved time resolution. The arrangement of Figure 2 includes the programmable delay 101, a selector 102, a microprocessor 103 for controlling the system as shown; delay elements 104 – 107 arranged with a delay locked loop 108, and a variety of interconnections between the foregoing elements. As further described, the circuit permits time resolution higher than the rate of clock 110 that is input into the arrangement.

In operation, a clock 110 and signal V_f are input into a programmable delay 101 that has been programmed to delay the input signal V_f by a specified number of clock cycles. 5 After the appropriate delay, an inverted delayed version of the signal V_f is placed upon output a_0 and fed sequentially through delay elements b_1-b_n . A delay locked loop 108 is connected to delay elements 104-107 and functions to maintain the entire delay through all of delay elements 104 – 107 to be a single clock cycle. Accordingly, each delay element (e.g. 105) delays the signal by $1/n$ of the clock cycle. Selector 102 may be configured via 10 microprocessor 103 to select one of its inputs for conveying to its output 112.

Once the signal V_f enters programmable delay 101, a delayed version of that signal is output onto each of the outputs $a_0 – a_n$. One of those outputs $a_0 – a_{n-1}$ is fed back through selector 112, causing an inverted version of the signal to be fed into programmable delay 101, and repeating the cycle all over. Thus, the signal V_f will oscillate and can be tuned at 15 resolutions higher than that of the clock frequency.

The time resolution of the circuit is thus not limited to the frequency of clock 110. Because the delay of all of elements 104 – 107 is a single clock cycle, the resolution achieved by selecting one of the delayed outputs is n times the resolution that the clock 110 would normally provide in prior art circuits. This is shown pictorially in Figure 3, where t_1 20 = the delay programmed into programmable delay 101, m is an index variable that ranges in value from 1 to n , and T is the period of V_f .

Figure 4 shows an alternative embodiment of the present invention for generating a pulse width modulated (PWM) signal. The system includes a programmable pulse width modulator circuit 401, a plurality of delay elements 402-405, a delay locked loop 4-6 similar 25 to that of Figure 2, a selector 408 for selecting one of inputs a_0 through a_n to the selector to convey to the selector output, and a logic gate 409 connected to the selector output. In operation, the programmable PWM outputs a PWM signal of a fixed duty cycle set in

accordance with instructions from microprocessor 14. The waveform that is output by programmable PWM generator 401 is shown as a_0 in Figure 5. In accordance with the inventions, the delay locked loop 406 maintains the delay of one full clock cycle through delay elements 402 – 405. Accordingly, each output is delayed by $1/n$ of the clock frequency, T_{clk} .

The selector 408 selects one of the inputs for conveyance to logic gate 409, which is shown as an OR gate. The output 411 will be on as long as either the PWN signal is on, or a delayed version of that signal remains on. Since the delayed version may be delayed by an amount that is less than the period of the clock, the PWM signal can have a time resolution n times not of the clock frequency.

Several exemplary relevant waveforms generated by the arrangement of Figure 4 are shown in Figure 5. a_0 represents the PWM signal produced directly at the output of programmable PWM 401. The second signal C represents a slightly delayed version of the signal that is conveyed through selector 408 as shown in Figure 4. The resulting PWM signal remains on for an amount of time that may be varied in increments of T_{clock}/n . The specific delay experienced depends upon which delay is selected by selector 408 in response to instructions from microprocessor 410. Delay locked loop 406 maintains the appropriate delays in each of delay elements 402 – 405 such that the delay can be controlled independent of temperature and process variations.

While the foregoing describes the preferred embodiment of the inventions, various other modifications or additions will be apparent to those who are skilled in the art. Such modification are intended to be covered by the claims appended hereto.